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SAMSUNG ELECTRONICS

Product Information

LEAD FREE

Product Information

SAMSUNG TFT-LCD

MODEL NO. : LTN141W1-L03

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LCD Product Planning Group 1, Marketing Team

Samsung Electronics Co . , LTD.

wise view™ SAMSUNG TFT-LCD

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GENERAL DESCRIPTION

DESCRIPTION

LTN141W1-L03 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching devices. This model is composed of a TFT LCD panel, a driver circuit and a backlight unit. The resolution of a 14.1" contains 1,280 x 800 pixels and can display up to 262,144 colors. 6 O'clock direction is the Optimum viewing angle.

FEATURES

- High contrast ratio, high aperture structure
- 1280 x 800 pixels resolution
- Low power consumption
- Fast Response
- Single CCFL
- DE(Data enable) only mode
- 3.3V LVDS Interface
- Onboard EEDID chip
- Green product (complied with RoHS requirement)

APPLICATIONS

- Notebook PC
- If the usage of this product is not for PC application, but for others, please contact SEC.

GENERAL INFORMATION

Item	Specification	Unit	Note
Display area	303.36(H) x 189.6(V) (14.1” diagonal)	mm	
Driver element	a-Si TFT active matrix		
Display colors	262,144		
Number of pixel	1280 x RGB(3) x 800	pixel	16 : 10
Pixel arrangement	RGB vertical stripe		
Pixel pitch	0.2370(H) x 0.2370(V) (TYP.)	mm	
Display Mode	Normally white		
Surface treatment	Haze 0(Glare),/25(Anti-glare), Hard-Coating 3H		

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MECHANICAL INFORMATION

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal (H)	319.0	319.5	320.0	mm	
	Vertical (V)	205.0	205.5	206.0	mm	
	Depth (D)	-	5.3	5.5	mm	(1)
Weight		-	425	440	g	

Note (1) Measurement condition of outline dimension
. Equipment : Vernier Calipers
. Push Force : 500g ·f (minimum)

1. ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

V_{DD} =3.3V, V_{SS} = GND = 0V

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	V	(1)
Logic Input Voltage	V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	V	(1)

Note (1) Within Ta (25 ± 2 °C)

(2) BACK-LIGHT UNIT

Ta = 25 ± 2 °C

Item	Symbol	Min.	Max.	Unit	Note
Lamp Current	I_L	2.0	7.0	mArms	(1)
Lamp frequency	F_L	40	80	kHz	(1)

Note 1) Permanent damage to the device may occur if maximum values are exceeded
Functional operation should be restricted to the conditions described under normal operating conditions.

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2. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state.
Measuring equipment : TOPCON BM-5A and PR-650

* Ta = 25 ± 2 °C, V_{DD}=3.3V, fv= 60Hz, f_{DCLK} = 68.9MHz, I_L = 6.0 mA

Item		Symbol	Condition	Min.	Typ.	Max	Unit
Contrast Ratio (5 Points)		CR	Normal Viewing Angle $\phi = 0$ $\theta = 0$	300	-	-	-
Response Time at Ta (Rising + Falling)		T_{RT}		-	25	35	msec
Average Luminance of White (5 Points)		$Y_{L,AVE}$		175	200	-	cd/m^2
Color Chromaticity (CIE)	Red	R_X		0.560	0.590	0.620	-
		R_Y		0.310	0.340	0.370	
	Green	G_X		0.290	0.320	0.550	
		G_Y		0.510	0.540	0.570	
	Blue	B_X		0.125	0.155	0.185	
		B_Y		0.110	0.140	0.170	
	White	W_X		0.285	0315	0.345	
		W_Y		0.300	0.330	0.360	
Viewing Angle	Hor.	θ_L	CR ≥ 10	40	45	-	Degrees
		θ_H		40	45	-	
	Ver.	ϕ_H		10	15	-	
		ϕ_L		25	30	-	
13 Points White Variation		δ_L		-	-	2.2	-

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3. ELECTRICAL CHARACTERISTICS

Product Information

3.1 TFT LCD MODULE

Ta= 25 ± 2°C

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Voltage of Power Supply		V_{DD}	3.0	3.3	3.6	V	
Differential Input Voltage for LVDS Receiver Threshold	High	V_{IH}	-	-	+100	mV	V_{CM} = +1.2V
	Low	V_{IL}	-100	-	-	mV	
Vsync Frequency		fv	-	60	-	Hz	
Hsync Frequency		f_H	-	48.96	-	KHz	
Main Frequency		f_{DCLK}	-	68.93	-	MHz	
Rush Current		I_{RUSH}	-	-	1.5	A	
Current of Power Supply	White	I_{DD}	-	290	-	mA	
	Mosaic		-	300	-	mA	
	V. Stripe		-	350	485	mA	

3.2 BACK-LIGHT UNIT

The backlight system is an edge-lighting type with a single CCFT (Cold Cathode Fluorescent Tube).
The characteristics of a single lamp are shown in the following table.

- INVERTER : SEM SIC 130T

Ta= 25 ± 2 °C

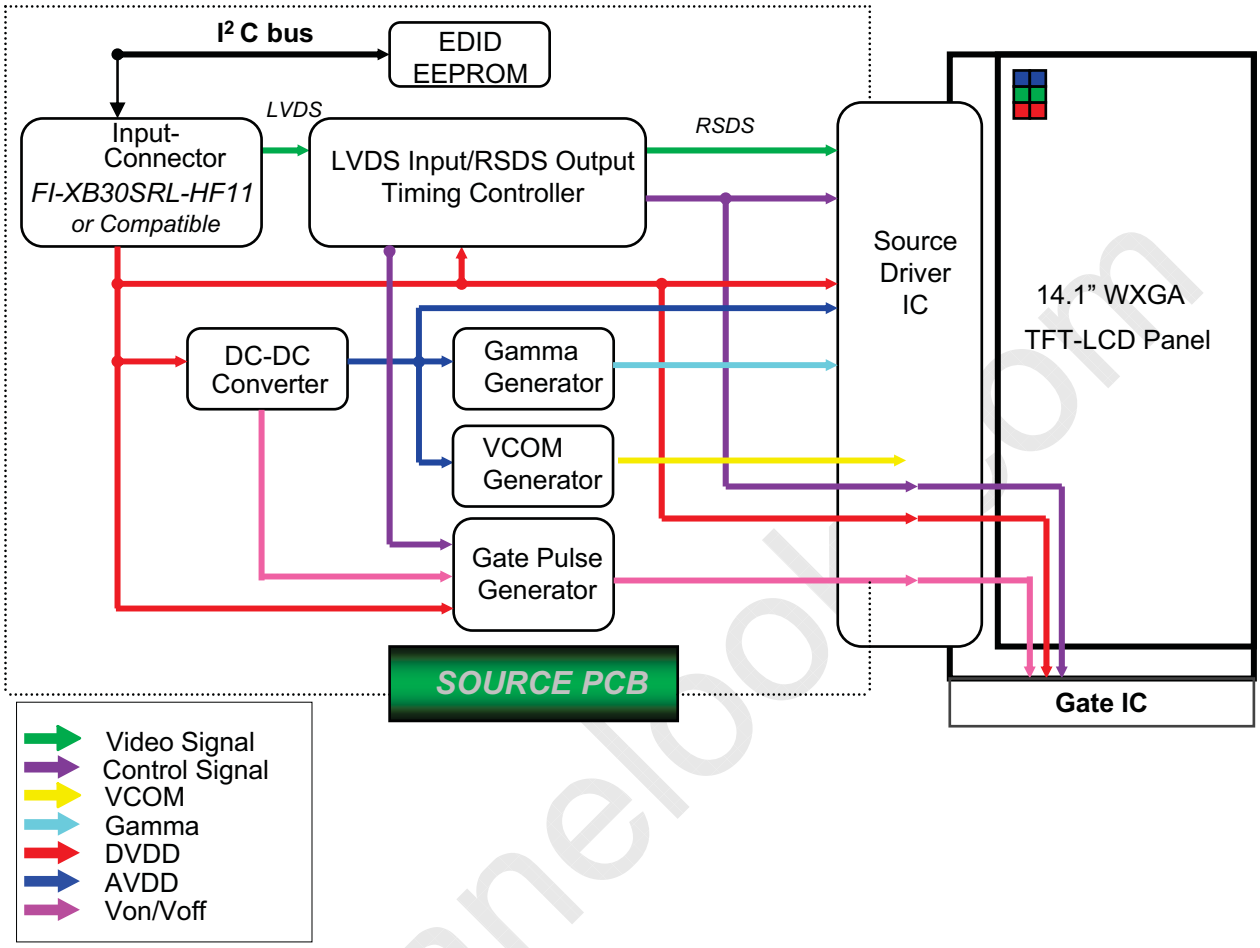
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Lamp Current	I_L	3.0	6.0	6.5	mArms	
Lamp Voltage	V_L	-	665	-	Vrms	I_L=6.0mA
Frequency	f_L	50	60	65	KHz	
Power Consumption	P_L		4.0		W	I_L=6.0mA
Operating Life Time	Hr	10,000			Hour	
Startup Voltage	V_S	-	-	1,120	Vrms	25°C
				1,345	Vrms	0°C
Lamp startup time		-	-	1.0	sec	

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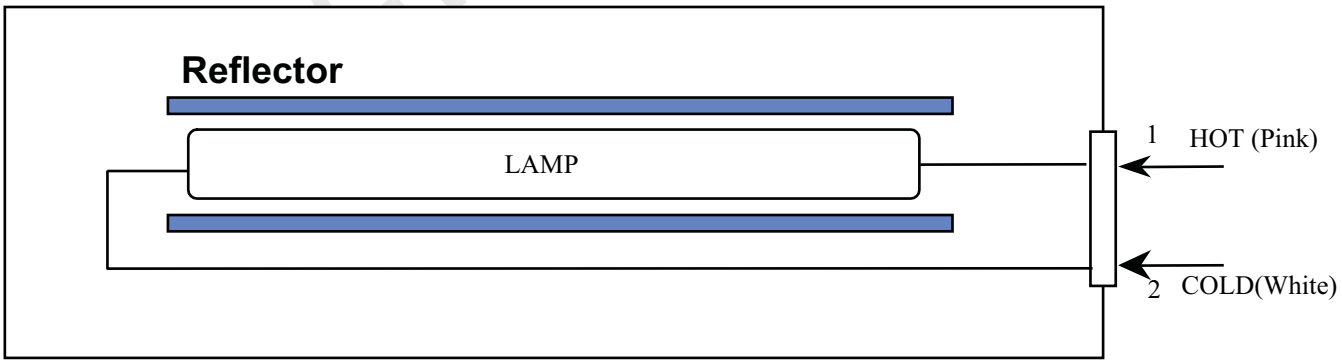
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4. BLOCK DIAGRAM

4.1 TFT LCD Module



4.2 BACK-LIGHT UNIT



Note) The output of the inverter may change according to the material of the reflector.

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5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power (LVDS, Connector : JAE FI-XB30SRL-HF11 or compatible)
Mating Connector : JAE FI-X30M or compatible)

No.	Symbol	Function	Polarity	Remarks
1	VSS	Ground		
2	VDD	POWER SUPPLY +3.3V		
3	VDD	POWER SUPPLY +3.3V		
4	VEEDID	DDC 3.3V Power		
5	NC	No connect		
6	CLKEDID	DDC Clock		
7	DATAEDID	DDC data		
8	RxIN0-	LVDS Differential Data INPUT (R0-R5,G0)	Negative	
9	RxIN0+	LVDS Differential Data INPUT (R0-R5,G0)	Positive	
10	GND	Ground		
11	RxIN1-	LVDS Differential Data INPUT (G1-G5,B0-B1)	Negative	
12	RxIN1+	LVDS Differential Data INPUT (G1-G5,B0-B1)	Positive	
13	GND	Ground		
14	RxIN2-	LVDS Differential Data INPUT (B2-B5,Sync,DE)	Negative	
15	RxIN2+	LVDS Differential Data INPUT (B2-B5,Sync,DE)	Positive	
16	Vss	Ground		
17	ClkIN-	LVDS Differential Clock INPUT	Negative	
18	ClkIN+	LVDS Differential Clock INPUT	Positive	
19	Vss	Ground		
20	NC	No connect		
21	NC	No connect		
22	NC	No connect		
23	NC	No connect		
24	NC	No connect		
25	NC	No connect		
26	NC	No connect		
27	NC	No connect		
28	NC	No connect		
29	NC	No connect		
30	NC	No connect		

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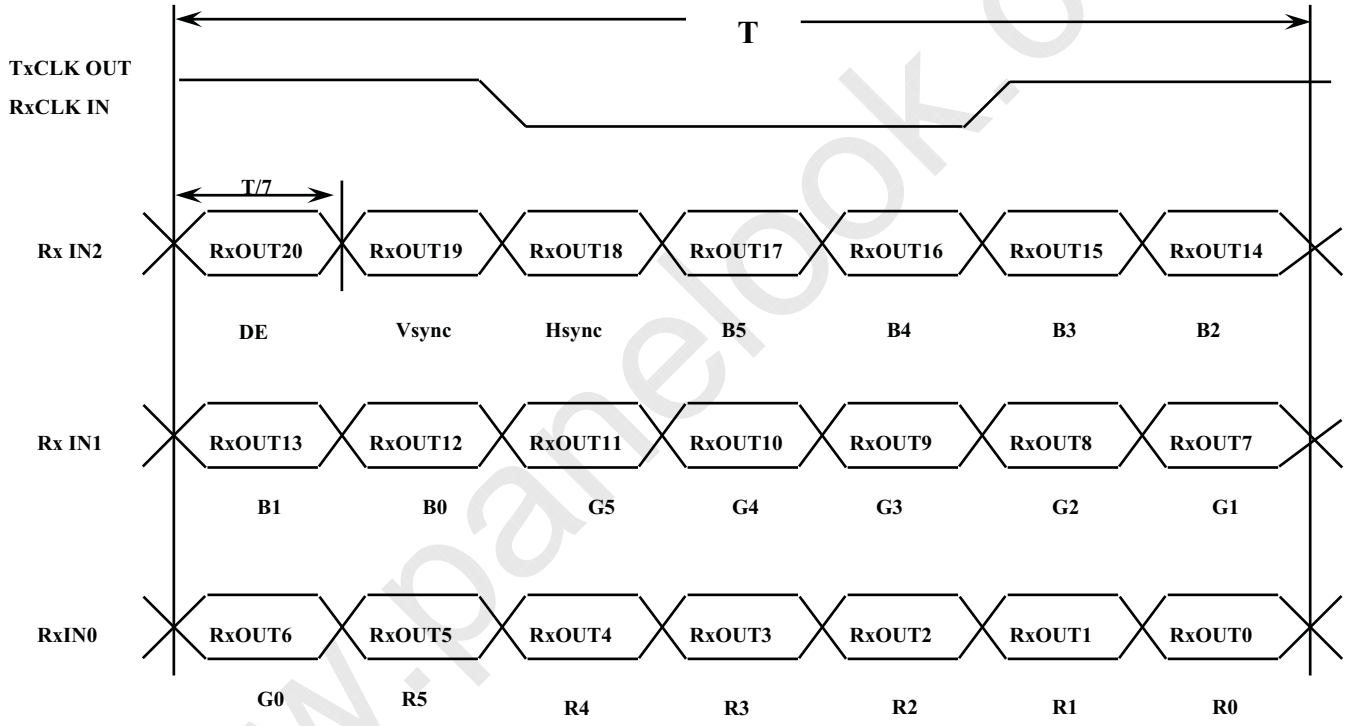
5.2 BACK LIGHT UNIT

Connector : JST BHSR - 02VS -1
Mating Connector : SM02B-BHSS-1(JST)

Pin NO.	Symbol	Color	Function
1	HOT	Pink	High Voltage
2	COLD	White	Low Voltage

5.3 Timing Diagrams of LVDS For Transmission

LVDS Receiver : Integrated T-CON



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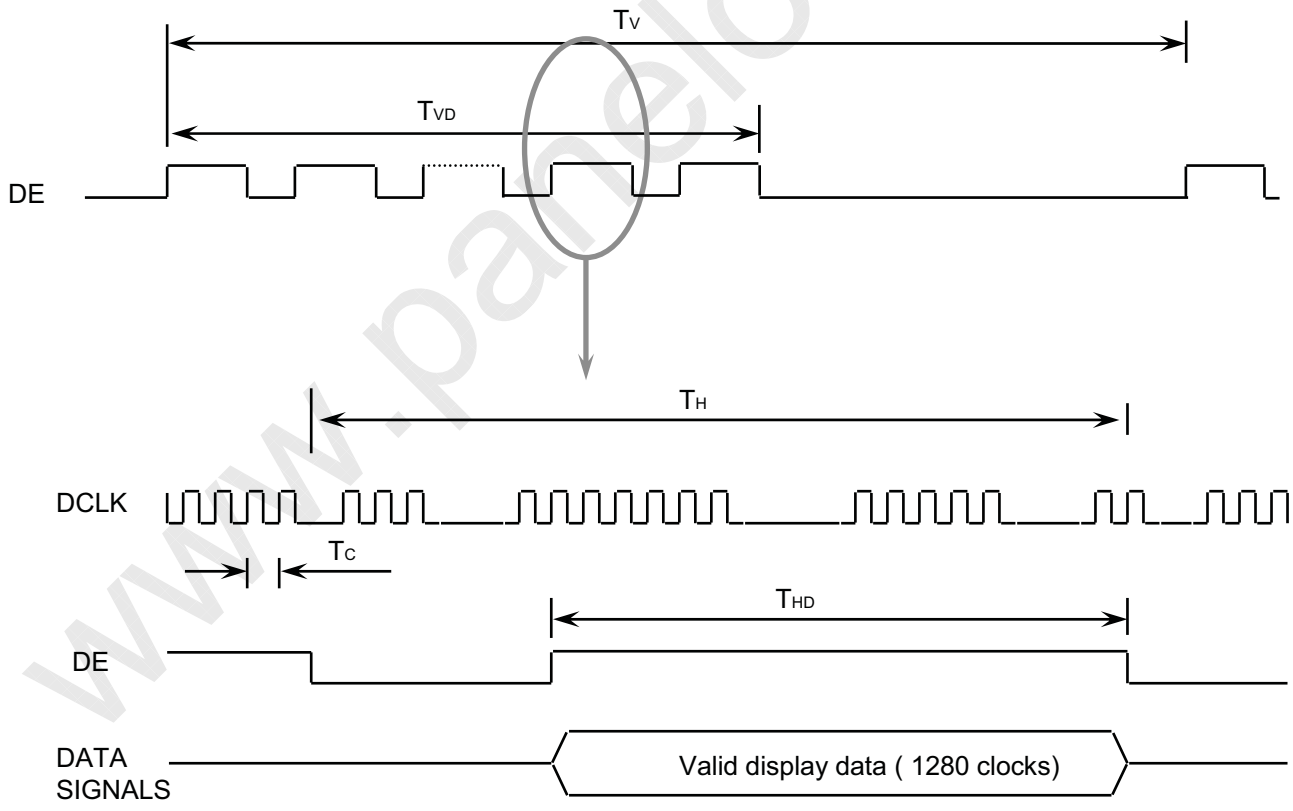
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6. INTERFACE TIMING

6.1 Timing Parameters

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frame Frequency	Cycle	TV	804	816	1000	Lines	-
Vertical Active Display Term	Display Period	TVD	-	800	-	Lines	-
One Line Scanning Time	Cycle	TH	1300	1408	1500	Clocks	-
Horizontal Active Display Term	Display Period	THD	-	1280	-	Clocks	-

6.2 Timing diagrams of interface signal



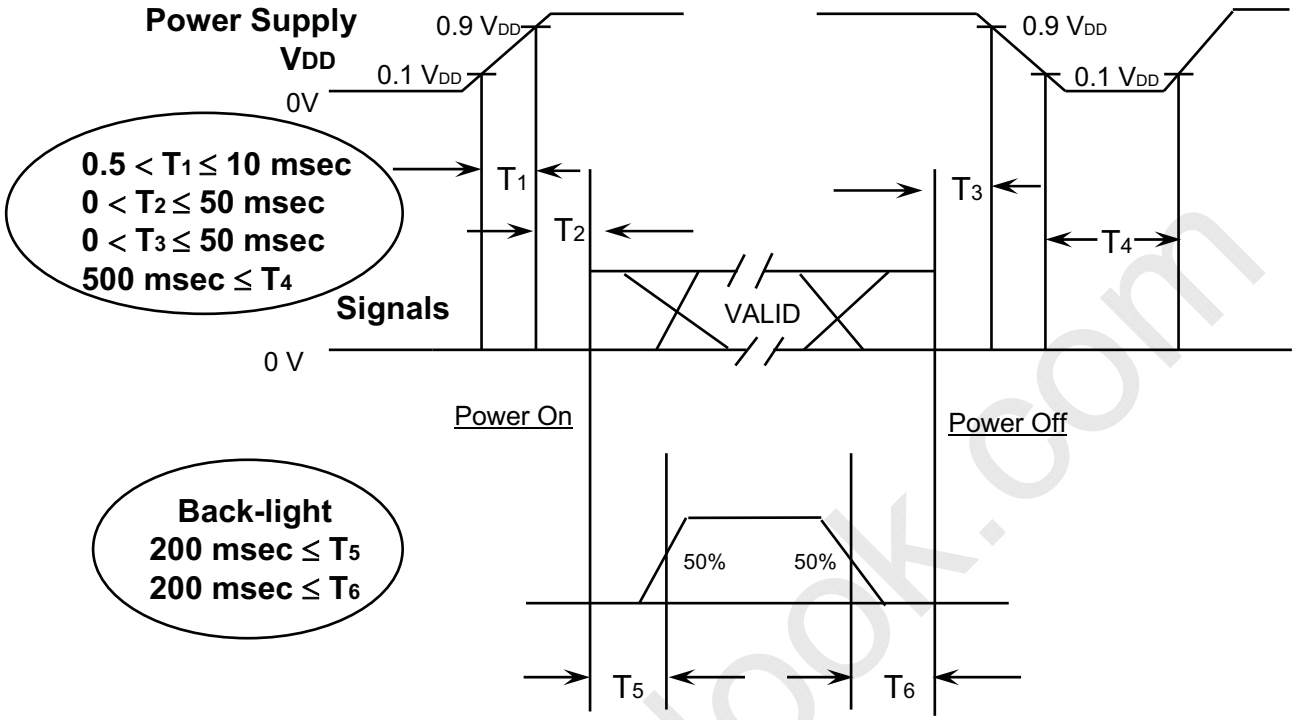
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6.3 Power ON/OFF Sequence

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: To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

T1 : Vdd rising time from 10% to 90%
T2 : The time from Vdd to valid data at power ON.
T3 : The time from valid data off to Vdd off at power Off.
T4 : Vdd off time for Windows restart
T5 : The time from valid data to B/L enable at power ON.
T6 : The time from valid data off to B/L disable at power Off.

NOTE.

(1) The supply voltage of the external system for the module input should be the same as the definition of VDD.

(2) Apply the lamp voltage within the LCD operation range. When the back-light turns on before the LCD operation or the LCD turns off before the back-light turns off, the display may momentarily become white.

(3) In case of VDD = off level, please keep the level of input signals on the low or keep a high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

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7. MECHANICAL OUTLINE DIMENSION

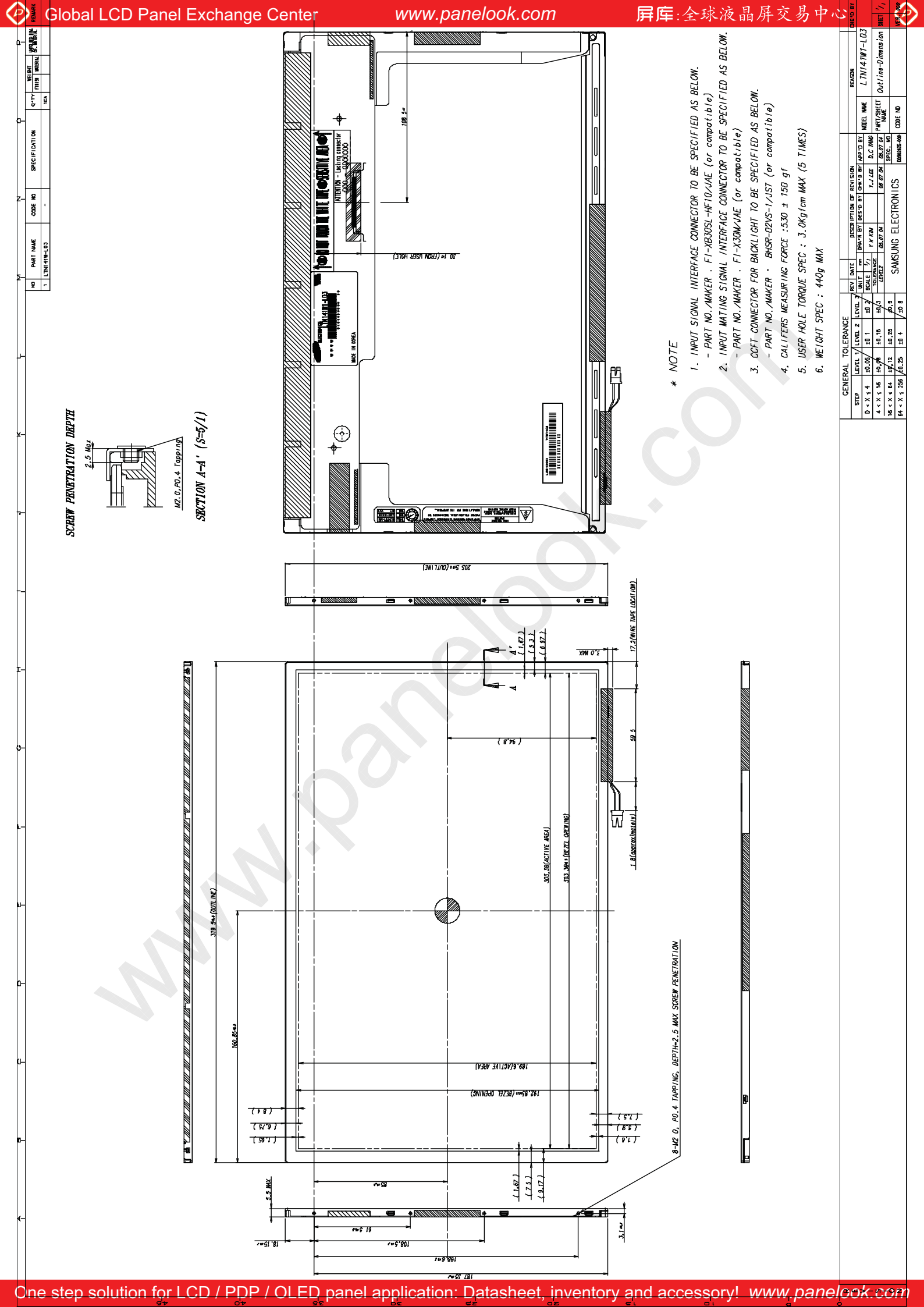
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NO	PART NAME	CODE NO	SPECIFICATION	Q'TY	WEIGHT	MATERIAL	REMARK
1	LTN141W1-L03	-		1EA			UNFOLDING BY MATERIAL

REV	DATE	DESCRIPTION OF REVISION	DRAW'N BY	DES'D BY	CHK'D BY	APP'D BY

GENERAL TOLERANCE						
STEP	LEVEL 1	LEVEL 2	LEVEL 3	UNIT	mm	
0 < X ≤ 4	±0.05	±0.1	±0.2	SCALE	1/1	
4 < X ≤ 16	±0.08	±0.15	±0.3	TOLERANCE LEVEL2		
16 < X ≤ 64	±0.12	±0.25	±0.5			
64 < X ≤ 256	±0.25	±0.4	±0.8			

MODEL NAME	LTN141W1-L03
PART/SHEET NAME	Outline Dimension
SPEC. NO	
CODE NO	0206A05-A00
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